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SNAP Clock Investigation

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1 Introduction

This memo summarizes the clock investigations in the Berkeley lab. We investigate some interesting phase noise as well as the effect of changing the synthesizer clock frequency on the phase noise.

2 Setup

A SNAP board with the lid off (serial C77) was running the 2021-03-03 snap fengine firmware, connected to a 10 MHz and 1 PPS from a white rabbit module. The tests were done using the hera_corr_f repository. We program the board, initialize the ADCs, align them, and set the LMX synthesizer frequency. We do not reinitialize the ADCs after changing the LMX, since the ADC code in hera_corr_f hardcodes the LMX chip to 500 MHz. We have a 13.45 MHz sine wave at +6 dBm going into SMA port E2 on the SNAP to use as an ADC sanity check. We check to made sure the ADC snapshot still looks reasonable after changing the LMX frequency, even without reinitializing, to make sure our further measurements are sensible.
The clock line data was taken on a Fieldfox spectrum analyzer, using a home-made sniffer probe shown in figure 1. The probe included a resistor such that the measurement is 20 dBm down from where the actual power is (add 20 dBm to all the plots in this memo for true power). The sniffer probe was placed at the clock line at U23 on the SNAP board. This is NOT the test point at TP2, but the actual clock that is distributed to the FPGA/ADCs.
The synthesizer frequencies tested were 500 MHz, 500.00038 MHz, and 500.021417 MHz. On a frequency counter locked to the white rabbit 10 MHz, the reported frequencies were 499.999999, 500.00037, and 500.021416, respectively. A probe of the sync period from the SNAP, or the number of FPGA clocks between PPS pulses, returns 250000000, 250000169, 250010708, respectively.

Figure 1: An image of the homemade sniffer probe used to make measurements of the clock line

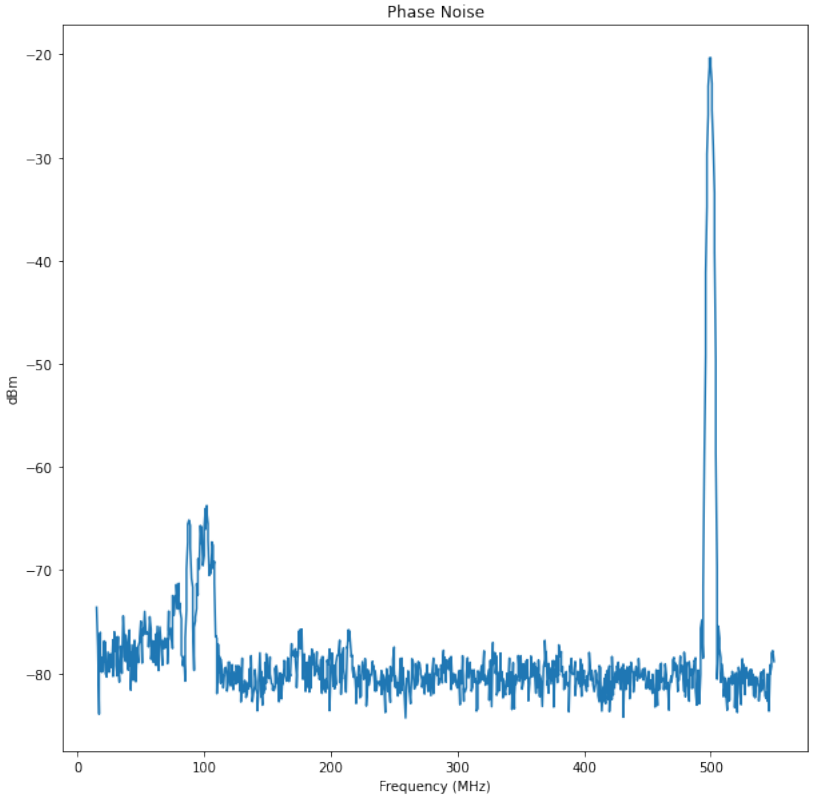

Figure 2: synth clock set to 500 MHz, extra phase noise shown at approximately 100 MHz

3 Results for extra phase noise investigation

This section shows the results for an investigation of some extra phase noise at 100 MHz. The plot in figure 2 shows our initial measurement with extra phase noise shown at approximately 100 MHz, with the synth clock set to 500 MHz. The plot in figure 3 shows our initial measurement with extra phase noise shown at approximately 100 MHz, with the synth clock set to 500 MHz, compared to a set of new measurements. These measurements have a manual grounding done by Matt, which appears to reduce the extra phase noise to a negligible level. The initial measurement is an 'ungrounded' (i.e, with the poor grounding) 500 MHz synth, and the other measurements are all done with the better grounding. This suggests that the extra noise may be a probe issue and the actual extra noise from the board is much lower.

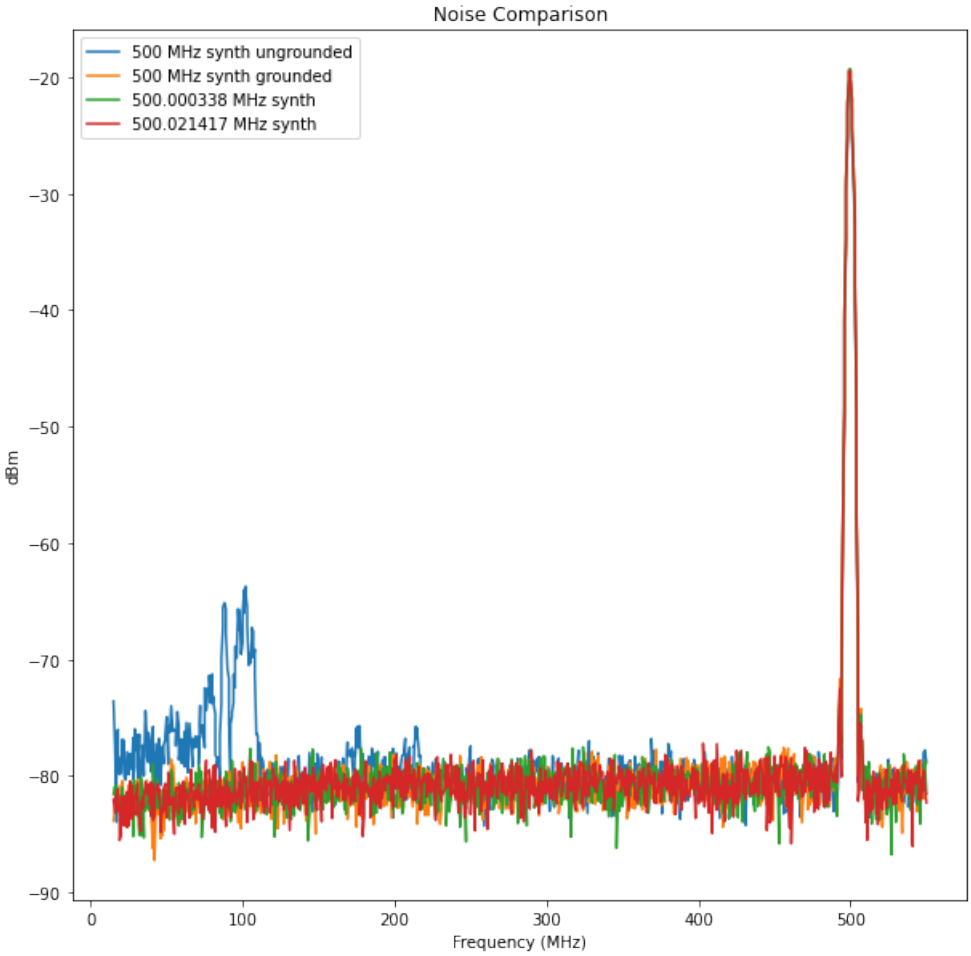

Figure 3: Initial measurement with extra phase noise shown at approximately 100 MHz, with the synth clock set to 500 MHz, compared to a set of new measurements with a better grounding on the probe to board and a few different clocks. All non 500 MHz measurements are grounded with the better grounding.

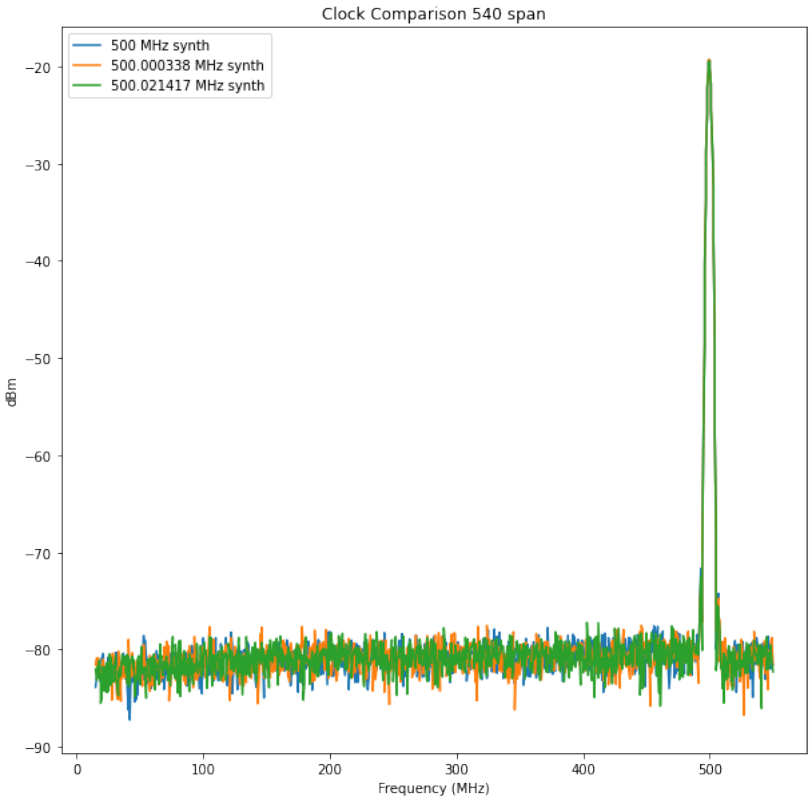

Figure 4: Frequency synthsizer outputs for a few different programmed frequencies. The differences are not appreciable at this span.

4 Results for synth freq test

After gaining confidence in our probe measurements, we moved on to testing the proposed change in clock frequencies for BDA. The clock frequencies were changed on the LMX synth chip, but NOT the ADC sampling rate. We checked to make sure the ADC voltages were sensible even with a sampling rate different than the LMX output frequencies, and visually there was no appreciable difference. Ideally the LMX output/ADC sampling rate will be the same, but the sampling rate parameter needs to be made accessible from the top level hera_corr_f code to do this. The results for this are shown at various frequency spans, with the clocks at 500 MHz, 500.000338 MHz, 500.021417 Mhz, with the ideally grounded probe, in figures 4, 5, 6, 7 . The results, especially in figure 7, show the expected increase in phase noise from changing the clock from the ideal 500 MHz, but suggest that the extra noise may be far enough down to avoid impacting science measurements.

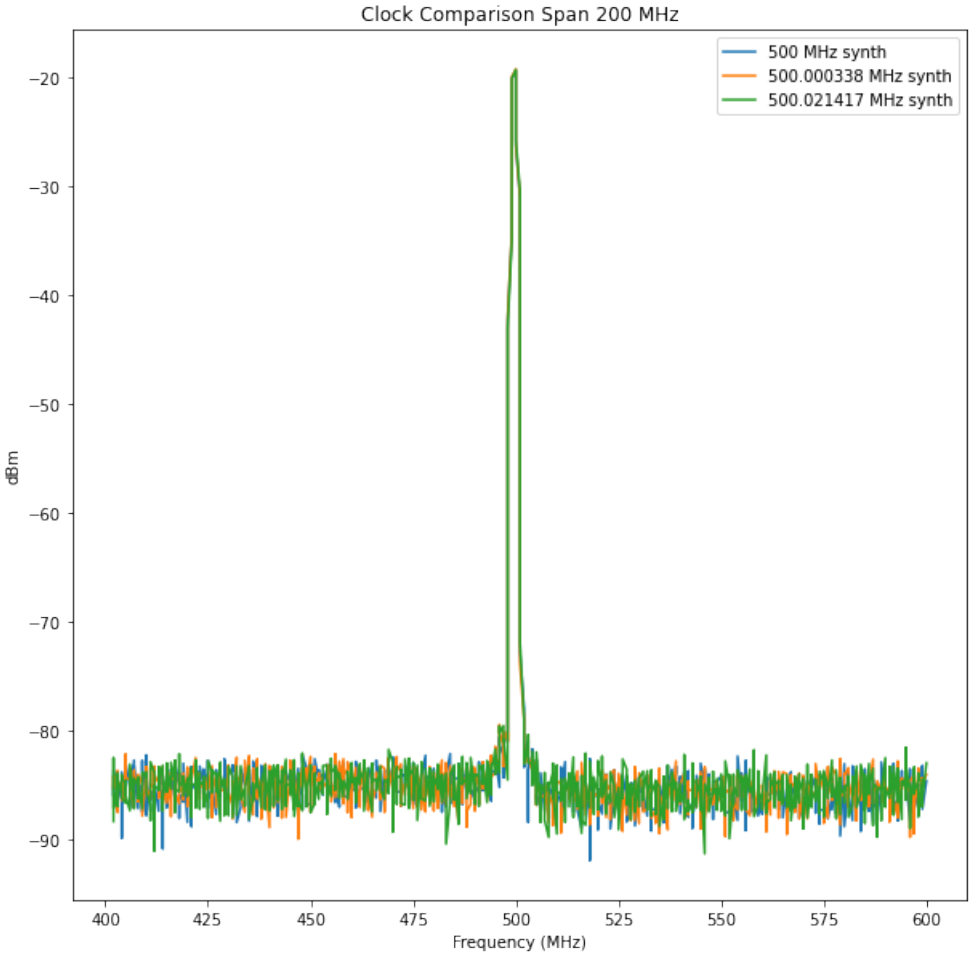

Figure 5: Frequency synthsizer outputs for a few different programmed frequencies. The differences are not appreciable at this span.

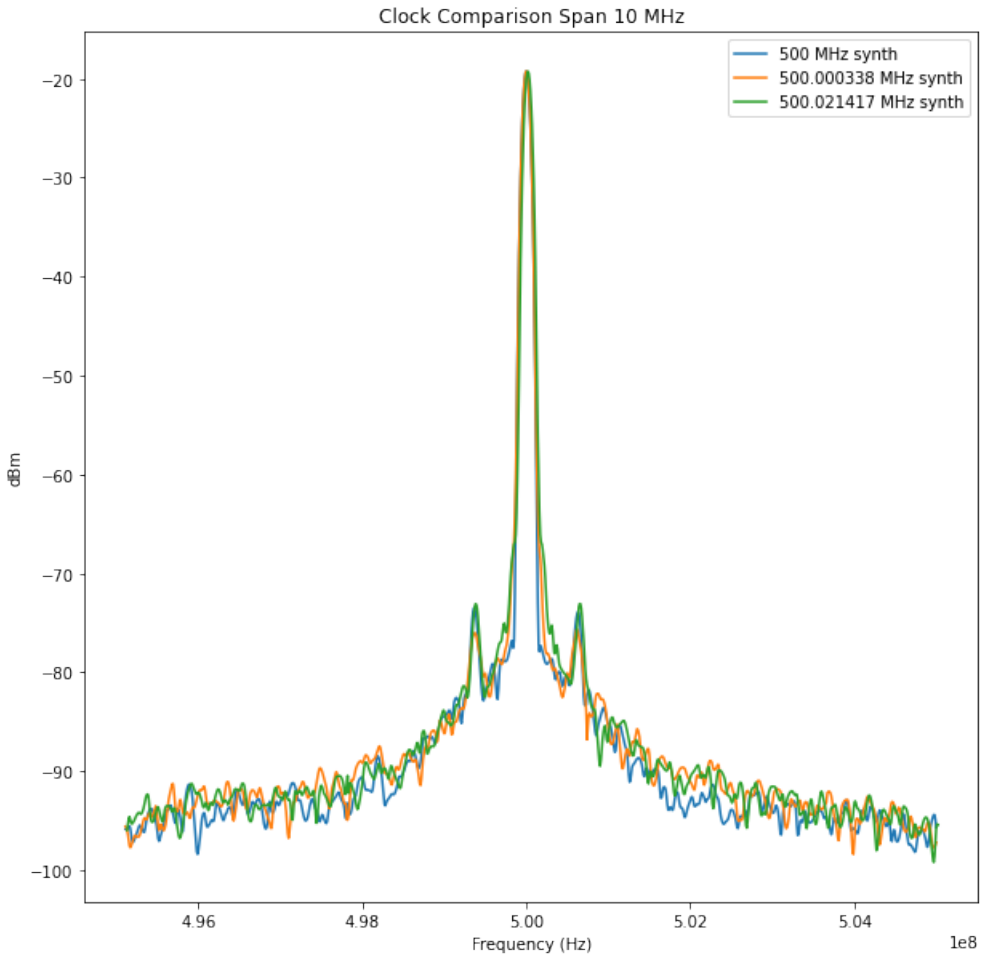

Figure 6: Frequency synthsizer outputs for a few different programmed frequencies. The differences are slight, but visible at this span. The 500.000338 shows larger shoulders and spikes than the 500, and the 500.021417 shows even larger differences. This is an expected result.

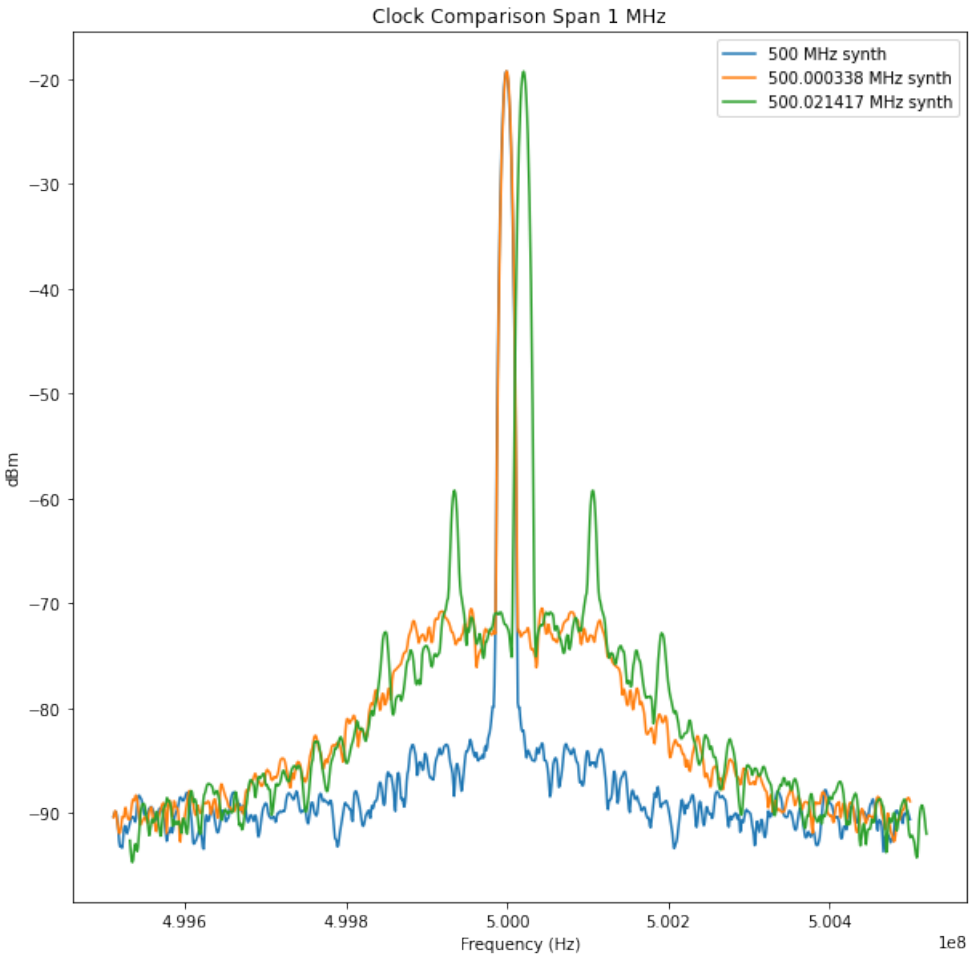

Figure 7: Frequency synthsizer outputs for a few different programmed frequencies. The differences are appreciable at this span. The 500.000338 shows much larger shoulders and spikes than the 500, and the 500.021417 shows even larger differences, especially in the spikes. This is an expected result.